AMENDMENT

IN THE CLAIMS:

Please amend the claims as follows:

1. (Canceled)

2. (Currently amended) The surface emitting semiconductor device according to ~~claim 1~~ claim 5, wherein III-V compound semiconductor of said active layer contains at least gallium (Ga) as a III group member; and

wherein said III-V compound semiconductor of said active layer further contains arsenic (As) as a V group member.

3. (Currently amended) The surface emitting semiconductor device according to ~~claim 1~~ claim 5, wherein said active layer is made of at least one of GaInNAs semiconductor; GaNAs semiconductor, GaNAsSb semiconductor, GaNAsP semiconductor, GaNAsSbP semiconductor, GaInNAsSb semiconductor, GaInNAsP semiconductor and GaInNAsSbP semiconductor.

4. (Currently amended) The surface emitting semiconductor device according to ~~claim 1~~ claim 5, wherein a refractive index of said second conductivity type semiconductor layer is higher than that of said current block semiconductor region.

5. (Currently amended) ~~The surface~~ A surface emitting semiconductor device ~~according to claim 1, further~~ comprising;

a first conductivity type semiconductor region having a side surface, said first conductivity type semiconductor region being provided on a GaAs semiconductor region;

an active layer having a side surface, said active layer being provided on said first conductivity type semiconductor region;

a second conductivity type semiconductor layer, provided on said active layer, and having a side surface;

a current block semiconductor region provided on said side surface of the first conductivity type semiconductor region, said side surface of said active layer, and said side surface of said second conductivity type semiconductor layer;

a first DBR portion having a plurality of first DBR semiconductor layers and a plurality of second DBR semiconductor layers, said first DBR semiconductor layers and said second DBR semiconductor layers being arranged alternately;

a second DBR portion having a plurality of third DBR semiconductor layers and a plurality of fourth DBR semiconductor layers, said third DBR semiconductor layers and said fourth DBR semiconductor layers being arranged alternately; and

an additional semiconductor layer made of III-V compound semiconductor;

wherein said first conductivity type semiconductor region, said active layer and said second conductivity type semiconductor layer are provided between said first DBR portion and said second DBR portion;

wherein said current block semiconductor region is provided for confining carriers to said first conductivity type semiconductor region, said active layer, and said second conductivity type semiconductor layer;

wherein said active layer is made of III-V compound semiconductor including at least a nitrogen element as a V group member;

wherein said additional semiconductor layer is provided between said active layer and said first conductivity type semiconductor region; and

wherein a photoluminescence wavelength of said III-V compound semiconductor of said additional semiconductor layer is between that of said active layer and that of said first conductivity type semiconductor region.

6. (Currently amended) ~~The surface~~ A surface emitting semiconductor device ~~according to claim 1, further~~ comprising;

a first conductivity type semiconductor region having a side surface, said first conductivity type semiconductor region being provided on a GaAs semiconductor region;

an active layer having a side surface, said active layer being provided on said first conductivity type semiconductor region;

a second conductivity type semiconductor layer, provided on said active layer, and having a side surface;

a current block semiconductor region provided on said side surface of the first conductivity type semiconductor region, said side surface of said active layer, and said side surface of second conductivity type semiconductor layer;

a first DBR portion having a plurality of first DBR semiconductor layers and a plurality of second DBR semiconductor layers, said first DBR semiconductor layers and said second DBR semiconductor layers being arranged alternately;

a second DBR portion having a plurality of third DBR semiconductor layers and a plurality of fourth DBR semiconductor layers, said third DBR semiconductor layers and said fourth DBR semiconductor layers being arranged alternately; and

an additional semiconductor layer made of III-V compound semiconductor;

wherein said first conductivity type semiconductor region, said active layer and said second conductivity type semiconductor layer are provided between said first DBR portion and said second DBR portion;

wherein said current block semiconductor region is provided for confining carriers to said first conductivity type semiconductor region, said active layer, and said second conductivity type semiconductor layer;

wherein said active layer is made of III-V compound semiconductor including at least one nitrogen element as a V group member;

wherein said additional semiconductor layer is provided between said active layer and said second conductivity type semiconductor layer; and

wherein a photoluminescence wavelength of said III-V compound semiconductor of said additional semiconductor layer is between that of said active layer and that of said second conductivity type semiconductor layer.

7. (Currently amended) ~~The surface~~ A surface emitting semiconductor device ~~according to claim 1, further~~ comprising:

a first conductivity type semiconductor region having a side surface, said first conductivity type semiconductor region being provided on a GaAs semiconductor region;

an active layer having a side surface, said active layer being provided on said first conductivity type semiconductor region;

a second conductivity type semiconductor layer, provided on said active layer, and having a side surface;

a current block semiconductor region provided on said side surface of the first conductivity type semiconductor region, said side surface of said active layer, and said side surface of said second conductivity type semiconductor layer;

a first DBR portion having a plurality of first DBR semiconductor layers and a plurality of second DBR semiconductor layers, said first DBR semiconductor layers and said second DBR semiconductor layers being arranged alternately;

a second DBR portion having a plurality of third DBR semiconductor layers and a plurality of fourth DBR semiconductor layers, said third DBR semiconductor layers and said fourth DBR semiconductor layers being arranged alternately;

a first SCH layer provided between said first conductivity type semiconductor region and said active layer; and

a second SCH layer provided between said active layer and said second conductivity type semiconductor layer;

wherein said first conductivity type semiconductor region, said active layer and said second conductivity type semiconductor layer are provided between said first DBR portion and said second DBR portion;

wherein said current block semiconductor region is provided for confining carriers to said first conductivity type semiconductor region, said active layer, and said second conductivity type semiconductor layer; and

wherein said active layer is made of III-V compound semiconductor including at least one nitrogen element as a V group member.

8. (Original) The surface emitting semiconductor device according to claim 7, further comprising an additional semiconductor layer made of III-V compound semiconductor;

wherein said additional semiconductor layer is provided between said first SCH layer and said first conductivity type semiconductor region; and

wherein a photoluminescence wavelength of said III-V compound semiconductor of said additional semiconductor layer is between that of said first SCH layer and that of said first conductivity type semiconductor layer.

9. (Original) The surface emitting semiconductor device according to claim 7, further comprising an additional semiconductor layer made of III-V compound semiconductor;

wherein said additional semiconductor layer is provided between said second SCH layer and said second conductivity type semiconductor layer;

wherein a photoluminescence wavelength of said III-V compound semiconductor of said additional semiconductor layer is between that of said second SCH layer and that of said second conductivity type semiconductor layer.

10. (Withdrawn, Currently amended) The surface emitting semiconductor device according to ~~claim 1~~ claim 5,

wherein said current block semiconductor region includes first and second current block layers;

wherein said first conductivity type semiconductor region is made of $(Al_{X1}Ga_{1-X1})_{Y1}In_{1-Y1}P$ semiconductor, where a composition X1 has a value in a range of zero or greater but not greater than 1;

wherein said second conductivity type semiconductor layer is made of $(Al_{X2}Ga_{1-X2})_{Y2}In_{1-Y2}P$ semiconductor, where a composition X2 has a value in a range of zero or greater but not greater than 1; and

wherein said first and second current block layers are made of $(Al_{X3}Ga_{1-X3})_{Y3}In_{1-Y3}P$ semiconductor, where a composition X3 has a value in a range of zero or greater but not greater than 1.

11. (Withdrawn, Currently amended) The surface emitting semiconductor device according to ~~claim 1~~ claim 5,

wherein said current block semiconductor region includes first and second current block layers;

wherein said first conductivity type semiconductor region is made of an $Al_{X1}Ga_{1-X1}As$ semiconductor, where a composition X1 has a value in a range of zero or greater but not greater than 1;

wherein said second conductivity type semiconductor layer is made of an $Al_{X2}Ga_{1-X2}As$ semiconductor, where a composition X2 has a value in a range of zero or greater but not greater than 1; and

wherein said first and second current block layers are made of $Al_{X3}Ga_{1-X3}As$ semiconductor, where a composition X3 has a value in a range of zero or greater but not greater than 1.

12. (Original) The surface emitting semiconductor device according to claim 7,

wherein said first SCH layer is made of one of $Al_{X1}Ga_{1-X1}As$ semiconductor ($0 \leq X1 \leq 1$) and $Ga_{X2}In_{1-X2}As_{Y2}P_{1-Y2}$ semiconductor (about $0.5 \leq X2 \leq 1$, $0 \leq Y2 \leq 1$) lattice-matched to GaAs semiconductor; and

wherein said second SCH layer is made of one of $Al_{X3}Ga_{1-X3}As$ semiconductor ($0 \leq X3 \leq 1$) and $Ga_{X4}In_{1-X4}As_{Y4}P_{1-Y4}$ semiconductor (about $0.5 \leq X4 \leq 1$, $0 \leq Y4 \leq 1$) lattice-matched to GaAs semiconductor.

13. (Currently amended) ~~The surface~~ A surface emitting semiconductor device ~~according to claim 1,~~ comprising:

a first conductivity type semiconductor region having a side surface, said first conductivity type semiconductor region being provided on a GaAs semiconductor region;

an active layer having a side surface, said active layer being provided on said first conductivity type semiconductor region;

a second conductivity type semiconductor layer, provided on said active layer, and having a side surface;

a current block semiconductor region provided on said side surface of the first conductivity type semiconductor region, said side surface of said active layer, and said side surface of second conductivity type semiconductor layer;

a first DBR portion having a plurality of first DBR semiconductor layers and a plurality of second DBR semiconductor layers, said first DBR semiconductor layers and said second DBR semiconductor layers being arranged alternately; and

a second DBR portion having a plurality of third DBR semiconductor layers and a plurality of fourth DBR semiconductor layers, said third DBR semiconductor layers and said fourth DBR semiconductor layers being arranged alternately;

wherein said first conductivity type semiconductor region, said active layer and said second conductivity type semiconductor layer are provided between said first DBR portion and said second DBR portion;

wherein said current block semiconductor region is provided for confining carriers to said first conductivity type semiconductor region, said active layer, and said second conductivity type semiconductor layer;

wherein said active layer is made of III-V compound semiconductor including at least one nitrogen element as a V group member;

wherein said current block semiconductor region includes first and second current block layers; and

wherein said first and second current block semiconductor layers are made of material not containing aluminum as a III group element.

14. (Currently amended) ~~The surface~~ A surface emitting semiconductor device ~~according to claim 1,~~ comprising:

a first conductivity type semiconductor region having a side surface, said first conductivity type semiconductor region being provided on a GaAs semiconductor region;

an active layer having a side surface, said active layer being provided on said first conductivity type semiconductor region;

a second conductivity type semiconductor layer, provided on said active layer, and having a side surface;

a current block semiconductor region provided on said side surface of the first conductivity type semiconductor region, said side surface of said active layer, and said side surface of said second conductivity type semiconductor layer;

a first DBR portion having a plurality of first DBR semiconductor layers and a plurality of second DBR semiconductor layers, said first DBR semiconductor layers and said second DBR semiconductor layers being arranged alternately; and

a second DBR portion having a plurality of third DBR semiconductor layers and a plurality of fourth DBR semiconductor layers, said third DBR semiconductor layers and said fourth DBR semiconductor layers being arranged alternately;

wherein said first conductivity type semiconductor region, said active layer and said second conductivity type semiconductor layer are provided between said first DBR portion and said second DBR portion;

wherein said current block semiconductor region is provided for confining carriers to said first conductivity type semiconductor region, said active layer, and said second conductivity type semiconductor layer;

wherein said active layer is made of III-V compound semiconductor including at least one nitrogen element as a V group member;

wherein said current block semiconductor region comprises first and second current block layers;

wherein said first and second current block semiconductor layers are made of material not containing aluminum as a III group element;

wherein said first conductivity type semiconductor region is made of material not containing aluminum as a III group element; and

wherein said second conductivity type semiconductor layer is made of material not containing aluminum as a III group element.

15. (Currently amended) The surface emitting semiconductor device according to ~~claim 1~~ claim 5,

wherein said GaAs semiconductor region is provided by one of a GaAs semiconductor layer and a gallium arsenide substrate.

16. (Currently amended) The surface emitting semiconductor device according to ~~claim 1~~ claim 5,

wherein said surface emitting semiconductor device is constituted to provide at least one of a semiconductor laser diode and a semiconductor optical amplifier.

17. (Currently amended) ~~The surface~~ A surface emitting semiconductor device ~~according to claim 1,~~ comprising:

a first conductivity type semiconductor region having a side surface, said first conductivity type semiconductor region being provided on a GaAs semiconductor region;

an active layer having a side surface, said active layer being provided on said first conductivity type semiconductor region;

a second conductivity type semiconductor layer, provided on said active layer, and having a side surface;

a current block semiconductor region provided on said side surface of the first conductivity type semiconductor region, said side surface of said active layer, and said side surface of said second conductivity type semiconductor layer;

a first DBR portion having a plurality of first DBR semiconductor layers and a plurality of second DBR semiconductor layers, said first DBR semiconductor layers and said second DBR semiconductor layers being arranged alternately; and

a second DBR portion having a plurality of third DBR semiconductor layers and a plurality of fourth DBR semiconductor layers, said third DBR semiconductor layers and said fourth DBR semiconductor layers being arranged alternately;

wherein said first conductivity type semiconductor region, said active layer and said second conductivity type semiconductor layer are provided between said first DBR portion and said second DBR portion;

wherein said current block semiconductor region is provided for confining carriers to said first conductivity type semiconductor region, said active layer, and said second conductivity type semiconductor layer;

wherein said active layer is made of III-V compound semiconductor including at least one nitrogen element as a V group member; and

wherein said GaAs semiconductor region is provided between said first DBR portion and said active layer.

18. (Currently amended) ~~The surface~~ A surface emitting semiconductor device ~~according to claim 1,~~ comprising:

a first conductivity type semiconductor region having a side surface, said first conductivity type semiconductor region being provided on a GaAs semiconductor region;

an active layer having a side surface, said active layer being provided on said first conductivity type semiconductor region;

a second conductivity type semiconductor layer, provided on said active layer, and having a side surface;

a current block semiconductor region provided on said side surface of the first conductivity type semiconductor region, said side surface of said active layer, and said side surface of said second conductivity type semiconductor layer;

a first DBR portion having a plurality of first DBR semiconductor layers and a plurality of second DBR semiconductor layers, said first DBR semiconductor layers and said second DBR semiconductor layers being arranged alternately; and

a second DBR portion having a plurality of third DBR semiconductor layers and a plurality of fourth DBR semiconductor layers, said third DBR semiconductor layers and said fourth DBR semiconductor layers being arranged alternately;

wherein said first conductivity type semiconductor region, said active layer and said second conductivity type semiconductor layer are provided between said first DBR portion and said second DBR portion;

wherein said current block semiconductor region is provided for confining carriers to said first conductivity type semiconductor region, said active layer, and said second conductivity type semiconductor layer;

wherein said active layer is made of III-V compound semiconductor including at least one nitrogen element as a V group member; and

wherein said second DBR portion is provided between said first DBR portion and said GaAs semiconductor region.

19-37. (Canceled)